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10/796,331	03/08/2004	David Meltzer	NP012	2121

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EXAMINER	
TORRES, JUAN A	
ART UNIT	**PAPER NUMBER**
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,331	MELTZER ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *13-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 03/26/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

The drawings are objected to because:

a) The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: D1 and D2 (figure 2, see page 6 lines 33-35); and Cf1, Cf2 and Rf1 (see page 12 line 37);

b) The recitation "7.6 KHz" in page 13 line 25 is improper, because to represent thousand a lower case k should be used; it is suggested to be changed to "7.6 kHz".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because exceed 150 words in length. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities:

a) The recitation in line 11 of page 2 "head room" is improper (see line 1 of page 2); it is suggested to be changed to "headroom";

b) The use of the trademark Cadence (see page 11 line 17); and Agilent (see page 14 line 9) have been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Appropriate correction is required.

Claim Objections

Claims 1-22 are objected to because of the following informalities:

Regarding claim 1 the recitation "comprising;" in line 1 is improper, because it is not properly constructed; it is suggested to be changed to "comprising:".

Regarding claims 2-22 they are objected because they depend directly or indirectly from claim 1, and claim 1 is objected.

Claims 13-22 are objected to because of the following informalities:

Regarding claim 13 the recitation "if" in lines 23, 26, 29 and 33 render the claim indefiniteness (35 USC § 112 2nd paragraph indefinite); it is clear what it happens if the condition is met, but if that condition is not met is indefinite. It is suggested to change the word "if" to "when".

Regarding claims 14-22 they are objected because they depend directly or indirectly from claim 13, and claim 13 is objected.

Regarding claim 14 the recitation "if" in line 5 of claim 14 render the claim indefiniteness (35 USC § 112 2nd paragraph indefinite); it is clear what it happens if the condition is met, but if that condition is not met is indefinite. It is suggested to change the word "if" to "when".

Regarding claim 15, the phrase "i.e." renders the claim indefinite because in colloquial English i.e. ("is est" or "that is" or "in other words") is commonly used as equivalent of e.g ("exempli gratia" or "for example"), and "for example" is indefinite under 35 USC § 112 second paragraph, because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d); it is suggested to change "i.e." to "that is".

Regarding claims 16-22 they are objected because they depend directly or indirectly from claim 15, and claim 15 is objected.

Regarding claim 19, the recitation "if" in lines 4, 7 and 10 render the claim indefiniteness (35 USC § 112 2nd paragraph indefinite); it is clear what it happens if the condition is met, but if that condition is not met is indefinite. It is suggested to change the word "if" to "when".

Regarding claims 20-22, they are objected because they depend directly from claim 19, and claim 19 is objected.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Messerschmitt ("Frequency Detectors for PLL Acquisition in Timing and Carrier

Recovery", IEEE Transactions on Communications, Publication Date: Sep 1979,Volume: 27, Issue: 9 page(s): 1288- 1295).

Regarding claim 1, Messerschmitt discloses a frequency synthesizer comprising an input node for receiving a reference frequency signal (figure 1 "input signal", section I page 1288 first column); a variable oscillator having a first control input and a second control input, and producing an oscillator output signal whose frequency is dependent on the first and second control inputs (figure 1 "VCO", section I page 1288); an analog voltage phase detector having a first phase-detection input responsive to the reference frequency signal and a second phase-detection input responsive to the oscillator output signal from the variable oscillator, the analog voltage phase detector being effective for producing a first control signal indicative of a phase difference between the reference frequency signal and the oscillator output signal, the first control signal being coupled to the first control input of the variable oscillator, where an analog loop is defined by the signal path along the first control signal from the analog voltage phase detector to the variable oscillator and along the oscillator output signal from the variable oscillator back to the analog voltage phase detector (figure 1 "phase detector", section I page 1288); a digital frequency difference detector having a first frequency-detection input responsive to the reference frequency signal and a second frequency-detection input responsive to the oscillator output signal, the digital frequency difference detector being effective for producing a second control signal indicative of a frequency difference between the reference frequency signal and the oscillator output signal, the second control signal being coupled to the second control input of the variable oscillator, where a digital loop

is defined by the signal path along the second control signal from the digital frequency difference detector to the variable oscillator and along the oscillator output signal from the variable oscillator back to the digital frequency detector (figure 1 "frequency detector", section I pages 1288-1289); where the bandwidth of the analog loop is greater than the bandwidth of the digital loop (section 3.5 page 1292 end of first paragraph).

Regarding claim 2, Messerschmitt discloses claim 1, Messerschmitt also discloses that the bandwidth of the analog loop is at least 200 times greater than the bandwidth of the digital loop (section 3.5 page 1292 end of first paragraph).

Regarding claim 3, Messerschmitt discloses claim 1, Messerschmitt also discloses that the variable oscillator is a voltage controlled oscillator (figure 1 "VCO", section I page 1288).

Regarding claim 4, Messerschmitt discloses claim 1, Messerschmitt also discloses a filter, where the first control signal is coupled to the first control input via the filter (figure 1 "loop filter Hp(s)", section 2 page 1289).

Regarding claim 11, Messerschmitt discloses claim 1, Messerschmitt also discloses the variable oscillator's first and second control inputs are independent of each other, and the variable oscillator has at least first and second frequency adjusting mechanisms separately responsive to the first and second control inputs, respectively (figure 1, section 1 pages 1288-1289).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Messerschmitt as applied to claim 1 above, and further in view of Moon (US 6114920 A) (see also Applicant's Admitted Prior Art in page 5 lines 16-32 and page 11 line 31 to page 12 line 9).

Regarding claim 5, Messerschmitt discloses claim 1, Messerschmitt doesn't specifically disclose a first frequency divider, where the input node for receiving the reference frequency signal is coupled to an input of the first frequency divider, and the output of the first frequency divider is coupled to the first phase-detection input of the analog voltage phase detector, whereby the first phase-detection input of the analog voltage phase detector is responsive to the reference frequency signal via the first frequency divider. Moon discloses a first frequency divider, where the input node for receiving the reference frequency signal is coupled to an input of the first frequency divider, and the output of the first frequency divider is coupled to the first phase-detection input of the analog voltage phase detector, whereby the first phase-detection input of the analog voltage phase detector is responsive to the reference frequency signal via the first frequency divider (figure 4 block 410 column 5 lines 11-26). Messerschmitt and Moon teachings are analogous art because they are from the same

field of endeavor of phase locked loops. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the system disclosed by Messerschmitt the frequency divider disclosed by Moon. The suggestion/motivation for doing so would have been to use PLL genus, which is known to those skilled in the art (Moon column 5 lines 11-26 and AAPA page 5 lines 16-32).

Regarding claim 6, Messerschmitt and Moon disclose claim 5, Moon also discloses that the output of the first frequency divider is coupled to the first frequency-detection input of the digital frequency difference detector, whereby the first frequency-detection input of the digital frequency difference detector is responsive to the reference frequency signal via the first frequency divider (figure 4 block 410 column 5 lines 11-26). Messerschmitt and Moon teachings are analogous art because they are from the same field of endeavor of phase locked loops. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the system disclosed by Messerschmitt the frequency divider disclosed by Moon. The suggestion/motivation for doing so would have been to use PLL genus, which is known to those skilled in the art (Moon column 5 lines 11-26 and AAPA page 5 lines 16-32).

Regarding claim 7, Messerschmitt discloses claim 1, Messerschmitt doesn't specifically disclose a second frequency divider having an input coupled to receive the oscillator output signal from the variable oscillator, and having an output coupled to the second phase-detection input of the analog voltage phase detector, whereby the second phase-detection input of the analog voltage phase detector is responsive to the oscillator output signal via the second frequency divider. Moon discloses a second

frequency divider having an input coupled to receive the oscillator output signal from the variable oscillator, and having an output coupled to the second phase-detection input of the analog voltage phase detector, whereby the second phase-detection input of the analog voltage phase detector is responsive to the oscillator output signal via the second frequency divider (figure 4 block 412 column 5 lines 11-26). Messerschmitt and Moon teachings are analogous art because they are from the same field of endeavor of phase locked loops. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the system disclosed by Messerschmitt the frequency divider disclosed by Moon. The suggestion/motivation for doing so would have been to use PLL genus, which is known to those skilled in the art (Moon column 5 lines 11-26 and AAPA page 5 lines 16-32).

Regarding claim 8, Messerschmitt and Moon disclose claim 7, Moon also discloses that the output of the second frequency divider is further coupled to the second frequency-detection input of the digital frequency difference detector, whereby the second frequency-detection input of the digital frequency difference detector is responsive to the oscillator output signal via the second voltage divider (figure 4 block 412 column 5 lines 11-26). Messerschmitt and Moon teachings are analogous art because they are from the same field of endeavor of phase locked loops. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the system disclosed by Messerschmitt the frequency divider disclosed by Moon. The suggestion/motivation for doing so would have been to use PLL genus,

which is known to those skilled in the art (Moon column 5 lines 11-26 and AAPA page 5 lines 16-32).

Regarding claim 9, Messerschmitt discloses claim 1, Messerschmitt doesn't specifically disclose that the second control signal from the digital frequency difference detector is coupled to the second control input of the variable oscillator via a digital-to-analog converter that provides the second control input an analog representation of the digital output from the digital frequency difference detector. Moon discloses that the second control signal from the digital frequency difference detector is coupled to the second control input of the variable oscillator via a digital-to-analog converter that provides the second control input an analog representation of the digital output from the digital frequency difference detector (figure 8 block 806 column 7 lines 26-37). Messerschmitt and Moon teachings are analogous art because they are from the same field of endeavor of phase locked loops. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the system disclosed by Messerschmitt the frequency divider disclosed by Moon. The suggestion/motivation for doing so would have been to use PLL genus, which is known to those skilled in the art (Moon column 5 lines 11-26 and AAPA page 11 line 31 to page 12 line 9).

Regarding claim 10, Messerschmitt and Moon disclose claim 9, Messerschmitt also the variable oscillator includes a summer for summing together the control signals at its first and second control inputs to produce a composite frequency control signal (figure 1 "summer", section I page 1288).

Regarding claim 12, Messerschmitt discloses claim 11, Messerschmitt doesn't specifically disclose that the variable oscillator's first and second control inputs are independent of each other, and the variable oscillator has at least first and second frequency adjusting mechanisms separately responsive to the first and second control inputs, respectively. Moon discloses that the variable oscillator's first and second control inputs are independent of each other, and the variable oscillator has at least first and second frequency adjusting mechanisms separately responsive to the first and second control inputs, respectively (figures 4 and 8 blocks C_{S2} and 804 column 5 lines 27-36 and column 7 lines 26-37). Messerschmitt and Moon teachings are analogous art because they are from the same field of endeavor of phase locked loops. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the system disclosed by Messerschmitt the frequency divider disclosed by Moon. The suggestion/motivation for doing so would have been to use PLL genus, which is known to those skilled in the art (Moon column 5 lines 11-26 and AAPA page 11 line 31 to page 12 line 9).

Allowable Subject Matter

Claims 13-22 are objected to as being dependent upon a rejected base claim, but would be allowable if the objections above are overcome and if they are rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: claims 13-22 are objected to because the references cited fail to teach, as

applicant has, a frequency synthesizer comprising an input node for receiving a reference frequency signal; a variable oscillator having a first control input and a second control input, and producing an oscillator output signal whose frequency is dependent on the first and second control inputs; an analog voltage phase detector having a first phase-detection input responsive to the reference frequency signal and a second phase-detection input responsive to the oscillator output signal from the variable oscillator, the analog voltage phase detector being effective for producing a first control signal indicative of a phase difference between the reference frequency signal and the oscillator output signal, the first control signal being coupled to the first control input of the variable oscillator, where an analog loop is defined by the signal path along the first control signal from the analog voltage phase detector to the variable oscillator and along the oscillator output signal from the variable oscillator back to the analog voltage phase detector; a digital frequency difference detector having a first frequency-detection input responsive to the reference frequency signal and a second frequency-detection input responsive to the oscillator output signal, the digital frequency difference detector being effective for producing a second control signal indicative of a frequency difference between the reference frequency signal and the oscillator output signal, the second control signal being coupled to the second control input of the variable oscillator, where a digital loop is defined by the signal path along the second control signal from the digital frequency difference detector to the variable oscillator and along the oscillator output signal from the variable oscillator back to the digital frequency detector; where the bandwidth of the analog loop is greater than the bandwidth of the digital loop, where

the digital frequency difference detector includes: an n-bit counter for counting pulses received at the first frequency-detection input, whereby the n-bit counter maintains a pulse-count of the reference frequency signal; an m-bit counter for counting pulses received at the second frequency detection input, whereby the m-bit counter maintains a pulse-count of the oscillation output signal, and where m is greater than n; a first memory cell for storing a SET condition in response to the nth bit within the m-bit counter transitioning into a first logic state and for maintaining the SET condition irrespective of the n^{th} bit within the m-bit counter transitioning out of the first logic state; a second memory cell for storing a SET condition in response to the $(n+1)^{th}$ bit within the m-bit counter transitioning into the first logic state and for maintaining the SET condition irrespective of the $(n+1)^{th}$ bit transitioning out of the first logic state; where the n-bit counter and the m-bit counter are halted in response to the n^{th} bit, within the n-bit counter transitioning into the first logic state; and where upon the halting of the n-bit and m-bit counters, the digital frequency difference detector determines: a) that the output frequency of the variable oscillator is lower than the reference frequency signal if neither of the first or second memory cells have the SET condition stored; or b) that the output frequency of the variable oscillator is higher than the reference frequency signal if the second memory cell has the SET condition stored; or c) that the output frequency of the variable oscillator is higher than the reference frequency signal if the first memory cell has the SET condition stored and any bit within the m-bit counter excluding a predetermined number of least significant bits is set to the first logic state; or d) that the output frequency of the variable oscillator is locked to the reference frequency signal if

the first memory cell has the SET condition stored and the second memory cell does not have the SET condition stored and no bit within the m-bit counter excluding the predetermined number of least significant bits is set to the first logic state, as the applicant has claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a) Lin (US 5446416 A) discloses a system architecture to achieve a fast time acquisition by utilizing independent dual-loop with frequency and phase locking operations capable of performing a continuous automatic frequency trimming;

b) McCollum (US 6028460 A) discloses a hybrid phase lock loop, which includes a digital component, an analog component and a loop monitor for switching between the digital control loop and the analog control loop;

c) Dosho (US 20010007436 A1) discloses a frequency detector and a phase-locked loop (PLL) circuit that can detect a frequency difference using the detector built in the circuit (see figure 4);

d) Brown (US 6826246 B1) discloses PLLs having control of the center frequency of the Voltage Controlled Oscillator (VCO) with the first divider, the second divider the first loop filter and the DAC (see figure 2); and

c) Dalmia (US 6310521 B1) discloses a conventional circuit 60 for performing clock and data recovery in a serial data communication device is shown that implements an analog phase detector and a digital frequency detector (see figure 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
6-26-2007